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PATENT APPLICATION

ATTORNEY DOCKET NO. 200302181-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): James Reuter

Application No.: 09/872,962

Filing Date: June 1, 2001

Confirmation No.: 4878

Examiner: Nawaz, Asad M.

Group Art Unit: 2152

Title: CENTRALIZED FINE-GRAINED ENHANCEMENTS FOR DISTRIBUTED TABLE DRIVEN I/O MAPPING

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 02/18/2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ [redacted]. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Typed Name: Jed Caven
Signature:

Respectfully submitted.

James Reuter
By

Jed Caven
Attorney/Agent for Applicant(s)

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Date : 11/03/2006

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Rev 10/05 (ApiBrief)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
James Reuter	)	Group Art Unit: 2152
	)	
Serial No.: 09/872,962	)	Examiner: Nawaz, Asad M.
	)	
Filing Date: June 1, 2001	)	Confirmation No.: 4878
	)	

For: CENTRALIZED FINE-GRAINED ENHANCEMENTS FOR DISTRIBUTED TABLE DRIVEN I/O MAPPING

SUPPLEMENTAL APPEAL BRIEF

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in response to the final rejections of the claims mailed February 8, 2006 and the Notice of Non-Compliant Appeal Brief mailed October 6, 2006. The undersigned attorney notes that the Notice of Appeal fee was paid with the previous Notice of Appeal filed July 6, 2005. Hence, no fee is due with the accompanying Notice of Appeal per MPEP 1207.04.

REAL PARTY IN INTEREST

The assignee of the entire right, title, and interest in the patent application is Hewlett-Packard Development Company.

RELATED APPEALS AND INTERFERENCES

There are currently no related appeals of other United States patent applications known to Appellants, Appellants' legal representative, or the assignee that will directly affect, or be directly affected by, or have a bearing on, the Board's decision. There are currently no related interferences known to Appellants, Appellants' legal representative, or the assignee which will directly affect, or be directly affected by, or have a bearing on, the Board's decision.

STATUS OF CLAIMS

Claims 1-16 are pending in the application. In the final Office Action mailed February 8, 2006, claims 1-11 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,940,850 to Harish, et al (hereinafter, "Harish"). Claims 12-16 were rejected under 35 U.S.C. §103(a) as being obvious over Harish in view of U.S. Patent No. 5,483,649 to Kuznetzov ("Kuznetzov").

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The subject matter of the independent claims is summarized below with reference numerals and reference to the specification and drawings in accordance with 37 CFR §41.37.

Claim 1

The subject matter recited in claim 1 is directed to a virtual storage system (page 4, lines 3-4; reference numeral 100) for mapping virtual storage segments of differing sizes to storage locations. In some embodiments, the system may comprise an agent (page 4, line 28 – page 6, line 13; reference numeral 110) coupled to the host (page 4, line 5; reference numeral 140), the agent (110). The agent may be embodied as a software module or a hardware module and may include volatile memory such as, e.g., DRAM that stores a first table (page 5, line 4; Fig. 2, reference numeral 200). The table includes entries to map virtual storage segments to storage locations. The subject matter in claim 1 further recites a controller (page 5, lines 20-31; Fig 1, reference numeral 120) coupled to the agent. In some embodiments the controller may have non-volatile memory for storing a second table (page 5, lines 20-31; reference numeral 201). The controller intermittently causes contents of the first table to be replaced by contents of the second table such that, during an input/output (I/O) operation, the host accesses one of the entries in the first table to determine one of the storage locations.

Claim 7

The subject matter recited in claim 7 is directed to a system (page 4, lines 3-4; reference numeral 100) for mapping a virtual disk segment to a storage location within a storage device (page 4, lines 10-15; reference numeral 160). In some embodiments, the system may comprise a first table (page 5, line 4; Fig. 2, reference numeral 200) having a first table entry (page 7, lines 11-20; reference numeral 210) mapping the virtual disk segment to the storage location. The system may further comprise a second table (page 5, lines 20-31; reference numeral 201) which has a second table entry (page 7, lines 11-20; reference numeral 210) corresponding to said storage location and to an alternate storage location, and block bitmap information identifying blocks of data having differing sizes within the alternate storage location (page 7, lines 11-29; reference numeral 225). The second data table may also maintain a plurality of variables indicating states of the entry (Figs. 2A-2B, , page 7, lines 19-page 14, line 15) and an offset for the entry, wherein the offset includes a logic unit number identifier and a block identifier (page 7, lines 9-10; reference numeral 234; page 11, lines 5-10; reference numeral 238). The system may further include a first memory (page 5, lines 8-12) to store the first table and a second memory (page 5, lines 25-30) to store the second table.

Claim 12

The subject matter recited in claim 12 is directed to a method for performing an input/output operation on a virtual storage segment defined by a first table (page 5, line 4; reference numeral 200) that maps the storage segment to a first storage location. In some embodiments, the method comprises the following operations.

Input/output operations are turned off at the first storage location. In some embodiments this is performed by activating the Nw state as described with reference to operation 310 in Fig. 3 at page 14, line 12 – page 15, and with reference to operation 429 at page 16, lines 10-20. In addition, the Quiesce function is described at page 19, line 26 – page 20, line 14.

Once input/output operations are quiesced, one or more portions of the virtual storage segment to be effected during the write operation are identified. For example, in one embodiment the controller may issue a fault message that includes the bitmap 225 designating the blocks in the segment that are to be changed, as described with reference to operation 720 at page 23, lines 3-10. This is described with reference to an embodiment which implements fine-grained mapping at page 23, lines 12-21. A record of the identified portions is stored at a second table and not at the first table. This is described with reference to a embodiment which implements fine-grained mapping at page 21, lines 22-30. Finally, a write operation may be directed to a second storage location, whereby the writing operation occurs at portions of the second storage location associated with the identified portions. In one embodiment, this may be implemented by the controller 120 ordering the mapping agent 110 to retry the I/O operation using an updated mapping table as described with reference to operation 585 at page 19, lines 1-10.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1-11 are anticipated under 35 U.S.C. §102(b) by U.S. Patent No. 5,940,850 to Harish, et al (hereinafter, "Harish").

2. Whether claims 12-16 are obvious under 35 U.S.C. §103(a) in view of Harish in view of Kuznetzov.

ARGUMENT

I. Rejections Under 35 U.S.C. §102

Claims 1-11 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,940,850 to Harish, et al (hereinafter, "Harish"). Applicants traverse these rejections.

The standard for lack of novelty, that is, for "anticipation," under 35 U.S.C. §102 is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements. *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 231 USPQ 81, 90 (Fed. Cir. 1986). Invalidity for anticipation requires that all of the elements and limitations of the claims be found within a single prior art reference. *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991). Every element of the claimed invention must be literally present, arranged as in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (finding that the jury had been erroneously instructed that anticipation may be shown by equivalents, a legal theory that is pertinent to obviousness under Section 103, not to anticipation under Section 102). "The identical invention must be shown in as complete detail as is contained in the patent claim." MPEP §2131 (7th Ed. 1998) (citing *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). Furthermore, functional language, preambles, and language in "whereby," "thereby," and "adapted to" clauses cannot be disregarded. *Pac-Tec, Inc. v. Amerace Corp.*, 14 USPQ2d 1871 (Fed. Cir. 1990).

"It is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office." *Ex parte Skinner*, 2 USPQ2d 1788, 1788-1789 (Bd. Pat. Int. 1986) (holding that examiner failed to establish *prima facie*

case of anticipation). The examiner has "the burden of proof . . . to produce the factual basis for its rejection of an application under sections 102 or 103." *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984) (quoting *In re Warner*, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967)). Only if that burden is met, does the burden of going forward shift to the applicant.

Claim 1

The final Action fails to establish a *prima facie* case that Harish anticipates independent claim 1. Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth in the manner recited in the claim in a single prior art reference. (See, MPEP 2131). Independent claim 1 recites structural elements including an agent, a host, and a controller coupled to the agent. The Action sets forth no evidence or argument that Harish discloses (or even suggests) structural elements corresponding to an agent, a host, and/or a controller coupled to the agent, as recited in claim 1. Therefore, the Action fails to establish a *prima facie* case of anticipation.

Further, Harish cannot anticipate (or render obvious) independent claim 1 because Harish neither discloses (nor even suggests) limitations recited in independent claim 1. Claim 1 recites "an agent coupled to a host, the agent having volatile memory for storing a first table, the table having entries to map the virtual storage segments to the storage locations; and a controller coupled to the agent, the controller having non-volatile memory for storing a second table, the controller intermittently causing contents of the first table to be replaced by contents of the second table." The Action asserts that Harish discloses this limitation, and cites the Abstract and column 2, lines 10-19 and 25-34 to support the rejection. Applicant disagrees. The cited text reads as follows:

A system and method for loading dynamic data stored in read-only memory (ROM) is loaded into random access memory (RAM) only when it is being modified. Unmodified dynamic data is used from ROM saving valuable RAM space. Virtual memory page table entries are created for all dynamic data with the physical reference pointing to the dynamic data in ROM. Page table entries in a translation table for dynamic data in ROM include a virtual address to physical address mapping and are marked read-only causing a write-access exception if an attempt is made to write to or update the dynamic data. Write-access exceptions are intercepted, and a write-access exception caused by an attempt to write to dynamic data in ROM causes the system to allocate a dynamic data page in RAM, copy the ROM data to the RAM, update the page table entry to point to the RAM page rather than the ROM page, and finally to update the dynamic data now present in read-write RAM.

ROM data is loaded into random access memory (RAM) only when that data is actually being modified. An attempt is detected to write to dynamic data in ROM and generates a write-access fault. The write-access fault is captured causing the system to copy the ROM data to RAM, change a page table entry to point to the RAM copy, and then write the data. This mechanism avoids loading ROM data that is not modified thereby reducing the RAM requirements for a given system.

The present invention is directed to a computer implemented method for loading read-only memory data into random access memory only when the data is modified, in a computer system having a processor, random access memory and read-only memory, comprising the steps of: storing a data page table entry for translating a virtual data address into physical data address for each dynamic data page; storing in the page table an indicator that-the page table entry is read-only if the physical data address is in read-only memory; receiving a write-access exception whenever the computer system attempts to write to a dynamic data page having a read-only indicator, and loading the read-only memory dynamic data page into random access memory in response to the write-access exception. The page table entry for the data page is then updated for future access by the system.

Nothing in this text discloses (or even suggests) an agent coupled to a host, the agent having volatile memory for storing a first table, the table having entries to map the virtual storage segments to the storage locations; and a controller coupled to the agent, the controller having non-volatile memory for storing a second table, the controller intermittently causing contents of the first table to be replaced by contents of the second table, as explicitly recited in claim 1. To the contrary, while claim 1 recites a controller that intermittently replaces the contents of a volatile memory to be replaced with the contents of a non-volatile memory, Harish describes precisely the opposite, i.e., updating the contents of a non-volatile memory with the contents of a volatile memory.

Claim 1 further recites that "during whereby during an input/output (I/O) operation, the host accesses one of the entries in the first table to determine one of the storage locations." The Action asserts that Harish discloses this limitation, and cites the Abstract and column 2, lines 12-34 to support the rejection. Applicant disagrees. Nothing in the cited text, which is excerpted above, discloses or suggests a host computer, much less a host computer that access an entry in a first table (i.e., a volatile memory table) to determine a storage location during an input/output (I/O) operation.

In sum, the Action fails to establish a *prima facie* case of anticipation. Furthermore, Harish fails to disclose or suggest elements of claim 1, and therefore cannot anticipate independent claim 1.

Claim 2

The final Action fails to establish a *prima facie* case that Harish anticipates independent claim 2. Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth in the manner recited in the claim in a single prior art reference. (See, MPEP 2131). Independent claim 2 recites limitations including "wherein the second table identifies an alternate storage location within the storage locations." The Action sets forth no evidence or argument that Harish discloses (or even suggests) an arrangement in which the second table identifies an alternate storage location within the storage locations, as recited in claim 2. Therefore, the Action fails to establish a *prima facie* case of anticipation.

Further, Harish cannot anticipate (or render obvious) independent claim 2 because Harish neither discloses (nor even suggests) limitations recited in independent claim 2. Claim 2 recites limitations including "wherein the second table identifies an alternate storage location within the storage locations." The Action asserts that Harish discloses this limitation, and cites the Abstract and column 2, lines 10-51 to support the rejection. Applicant disagrees. The cited text reads as follows:

> ROM data is loaded into random access memory (RAM) only when that data is actually being modified. An attempt is detected to write to dynamic data in ROM and generates a write-access fault. The write-access fault is captured causing the system to copy the ROM data to RAM, change a page table entry to point to the RAM copy, and then write the data. This mechanism avoids loading ROM data that is not modified thereby reducing the RAM requirements for a given system.
>
> The present invention is directed to a computer implemented method for loading read-only memory data into random access memory only when the data is modified, in a computer system having a processor, random access memory and read-only memory, comprising the steps of: storing a data page table entry for translating a virtual data address into physical data address for each dynamic data page; storing in the page table an indicator that-the page table entry is read-only if the physical data address is in read-only memory; receiving a write-access exception whenever the computer system attempts to write to a dynamic data page having a read-only indicator, and loading the read-only memory dynamic data page into random access memory in response

to the write-access exception. The page table entry for the data page is then updated for future access by the system.

It is therefore an object of the present invention to provide an apparatus and method for loading dynamic data from ROM to RAM only when that data is to be modified.

It is yet another object of the invention to provide an apparatus and method for using ROM dynamic data for execution unless that data is modified.

It is yet another object of the invention to provide an apparatus and method for enabling use of dynamic data in ROM without modifying the application program or base operating system function.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings wherein like reference numbers represent like parts of the invention.

Nothing in this text discloses (or even suggests) wherein the second table identifies an alternate storage location within the storage locations, as recited in claim 2. Therefore, Harish cannot anticipate claim 2.

Claim 3

The final Action fails to establish a *prima facie* case that Harish anticipates independent claim 3. Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth in the manner recited in the claim in a single prior art reference. (See, MPEP 2131). Independent claim 3 recites limitations including "the second table further includes a bitmap having entries that correspond to blocks of data stored within the alternate storage location." The Action sets forth no evidence or argument that Harish discloses (or even suggests) an arrangement in which the second table further includes a bitmap having entries that correspond to blocks of data stored within the alternate storage location, as recited in claim 3. Therefore, the Action fails to establish a *prima facie* case of anticipation.

Further, Harish cannot anticipate (or render obvious) independent claim 3 because Harish neither discloses (nor even suggests) limitations recited in independent claim 3. Claim 3 recites limitations including "the second table further includes a bitmap having entries that correspond to blocks of data stored within the alternate storage location." The Action asserts that Harish discloses this limitation, and cites the Abstract and column 2, lines 10-51 to support the rejection. Applicant disagrees. Nothing in this text discloses (or even suggests) an arrangement in which the second table identifies an alternate storage location within the storage locations, as recited in claim 3. Therefore, Harish cannot anticipate claim 3.

Claim 4

The final Action fails to establish a *prima facie* case that Harish anticipates independent claim 4. Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth in the manner recited in the claim in a single prior art reference. (See, MPEP 2131). Independent claim 4 recites limitations including "an alternate storage container comprising alternate storage locations of the storage location correlating to the virtual storage segments." The Action sets forth no evidence or argument that Harish discloses (or even suggests) an arrangement in which an alternate storage container comprising alternate storage locations of the storage location correlating to the virtual storage segments, as recited in claim 4. Therefore, the Action fails to establish a *prima facie* case of anticipation.

Further, Harish cannot anticipate (or render obvious) independent claim 4 because Harish neither discloses (nor even suggests) limitations recited in independent claim 4. Claim 4 recites limitations including "an alternate storage container comprising alternate storage locations of the storage location correlating to the virtual storage segments." The Action asserts that Harish discloses this limitation, and cites the Abstract and column 2, lines 10-51 to support the rejection. Applicant disagrees. Nothing in this text discloses (or even suggests) an arrangement in which an alternate storage container comprising alternate storage locations of the storage location correlating to the virtual storage segments, as recited in claim 4. Therefore, Harish cannot anticipate claim 4.

Claim 5

The final Action fails to establish a *prima facie* case that Harish anticipates independent claim 5. Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth in the manner recited in the claim in a single prior art reference. (See, MPEP 2131). Independent claim 5 recites limitations including "an I/O operation accesses information on both the storage location and the alternative storage location." The Action sets forth no evidence or argument that Harish discloses (or even suggests) an arrangement in which an I/O operation accesses information on both the storage location and the alternative storage location, as recited in claim 5. Therefore, the Action fails to establish a *prima facie* case of anticipation.

Further, Harish cannot anticipate (or render obvious) independent claim 5 because Harish neither discloses (nor even suggests) limitations recited in independent claim 5. Claim 5 recites limitations including "an I/O operation accesses information on both the storage location and the alternative storage location." The Action asserts that Harish discloses this limitation, and cites the Abstract and column 2, lines 10-51 to support the rejection. Applicant disagrees. Nothing in this text discloses (or even suggests) an arrangement in which an I/O operation accesses information on both the storage location and the alternative storage location, as recited in claim 5. Therefore, Harish cannot anticipate claim 5.

Claim 6

The final Action fails to establish a *prima facie* case that Harish anticipates independent claim 6. Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth in the manner recited in the claim in a single prior art reference. (See, MPEP 2131). Independent claim 6 recites limitations including "a bitmap designates blocks at the alternative storage location to use for the I/O operation." The Action sets forth no evidence or argument that Harish discloses (or even suggests) an arrangement in which a bitmap designates blocks at the alternative storage location to use for the I/O operation, as recited in claim 6. Therefore, the Action fails to establish a *prima facie* case of anticipation.

Further, Harish cannot anticipate (or render obvious) independent claim 6 because Harish neither discloses (nor even suggests) limitations recited in independent claim 6. Claim 6 recites limitations including "a bitmap designates blocks at the alternative storage location to use for the I/O operation." The Action asserts that Harish discloses this limitation, and cites the Abstract and column 2, lines 10-51 to support the rejection. Applicant disagrees. Nothing in this text discloses (or even suggests) an arrangement in which a bitmap designates blocks at the alternative storage location to use for the I/O operation, as recited in claim 6. Therefore, Harish cannot anticipate claim 6.

Claim 7

The final Action fails to establish a *prima facie* case that Harish anticipates independent claim 7. Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth in the manner recited in the claim in a single prior art reference. (See, MPEP 2131). Independent claim 7 recites:

> 7. A system for mapping a virtual disk segment to a storage location within a storage device, such that a host queries said system to determine said storage location for input/output operations, said system comprising:
> a first table having a first table entry mapping the virtual disk segment to the storage location;
> a second table having a second table entry corresponding to said storage location and to an alternate storage location, and block bitmap information identifying blocks of data having differing sizes within the alternate storage location;
> a plurality of variables indicating states of an entry in the first table or the second table;
> an offset for the entry, wherein the offset includes a logic unit number identifier and a block identifier;
> a first memory to store the first table; and
> a second memory to store the second table.

The final Action fails to provide any citation to relevant portions of Harish to support the assertion that Harish discloses limitations of claim 7, instead asserting that "[claim] 7 is essentially the system claim for claim 1. The Action sets forth no evidence or argument that Harish discloses (or even suggests) structural elements corresponding to a first table having a first table entry mapping the virtual disk segment to the storage location, and a second table having a second table entry corresponding to said storage location and to an alternate storage location, and block bitmap information identifying blocks of data having differing sizes within the alternate storage location, as recited in claim 7. Therefore, the Action fails to establish a *prima facie* case of anticipation.

Further, Harish cannot anticipate (or render obvious) independent claim 7 because Harish neither discloses (nor even suggests) limitations recited in independent claim 7. Claim 7 recites

"a plurality of variables indicating states of an entry in the first table or the second table, and an offset for the entry, wherein the offset includes a logic unit number identifier and a block identifier" The Action asserts that Harish discloses this limitation, and cites Fig. 3, column 4, lines 20-37; column 2, lines 19-51 and column 3, lines 56-67 to support the rejection. Applicant disagrees. The cited text reads as follows:

> ROM data is loaded into random access memory (RAM) only when that data is actually being modified. An attempt is detected to write to dynamic data in ROM and generates a write-access fault. The write-access fault is captured causing the system to copy the ROM data to RAM, change a page table entry to point to the RAM copy, and then write the data. This mechanism avoids loading ROM data that is not modified thereby reducing the RAM requirements for a given system.
>
> Virtual memory management systems separate the logical system memory reference from the physical address of the referenced object. This allows the system to reference a greater amount of memory than is physically present in a system. Virtual memory management schemes typically are based on pages of memory. At any point in time a number of pages are present in memory. These pages are tracked using a page table that cross references the virtual address to the location of the actual page containing the memory data. If an address reference is requested that does not exist in the page table, a page fault occurs requiring the referenced page to be loaded into memory. Memory pages are typically managed on a least recently used basis. The system will discard the least recently used page in memory and replace it with the one requested. If necessary, the page to be discarded is written out to storage before the page is freed.
>
> The present invention adds logic to the routine for handling write-access exceptions or faults. The flowchart of FIG. 3 illustrates the process flow for handling write-access faults for dynamic data resident in ROM. The process begins at the start block 301. The system then raises a write-access fault at step 306 when an attempt is made to modify a piece of dynamic data at step 302. After an attempt to write dynamic data is made at step 302, a query is made of whether a page table entry (PTE) exists at block 303. If yes, the process continues to step 304 to be hereinafter described. If no PTE entry exists, flow exits to the right of block 303, indicating a process page fault at block 305 and the process returns to block 303. The system tests in step 304 to determine whether the page table entry PTE protection is "read-only". If not, the data is written at step 316 using known processes. If the entry is "read-only" a "write-access fault" is raised at step 306.

Nothing in this text discloses (or even suggests) a plurality of variables indicating states

of an entry in the first table or the second table, and an offset for the entry, wherein the offset includes a logic unit number identifier and a block identifier, as recited in claim 7. To the contrary, Harish fails even to mention a logical unit, a logical unit number identifier, or a block identifier.

In sum, the Action fails to establish a *prima facie* case of anticipation. Furthermore, Harish fails to disclose or suggest elements of claim 7, and therefore cannot anticipate independent claim 7.

Rejections Under 35 U.S.C. §103

Claims 12-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Harish in view of U.S. Patent No. 5,483,649 to Kuznetzov (hereinafter, "Kuznetzov"). Applicant traverses this rejection, and asserts that the final Action fails to establish a *prima facie* case of obviousness.

Claim 12

Applicant traverses the rejection of claim 12 and assert that the final Action fails to establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, the Action must establish that each element of the claim is disclosed or suggested by the cited references. *See*, MPEP 2142.

Independent claim 12 includes a limitation reciting "identifying portions of the virtual storage segment to be effected during a write operation." The Action asserts that Harish discloses this limitation, and cites column 2 lines 19-51 and column 3, lines 56-67 to support the assertion. Applicants disagree. Contrary to the assertion in the action, nothing in the cited text, excerpted above, discloses or suggests *identifying portions of the virtual storage segment to be effected during a write operation*, as recited in claim 12.

Claim 12 further recites limitations requiring "storing a record of the identified portions at a second table and not at the first table" and "writing to a second storage location, whereby the writing operation occurs at portions of the second storage location associated with the identified portions." The Action asserts that Harish discloses this limitation, and cites column 2 lines 19-51 and column 3, lines 56-67 to support the assertion. Applicants disagree. Contrary to the assertion in the action, nothing in the cited text, excerpted above, discloses or suggests storing a record of the identified portions at a second table and not at

the first table and writing to a second storage location, whereby the writing operation occurs at portions of the second storage location associated with the identified portions," as recited in claim 12.

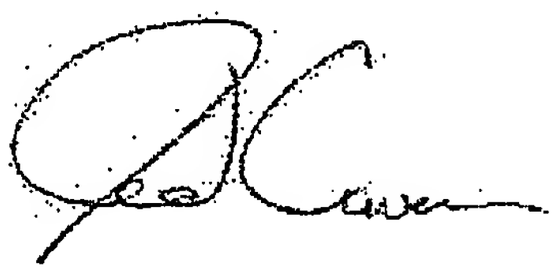
CONCLUSIONS

The final Action fails to provide an evidentiary record sufficient to support an anticipation rejection of claims 1-11 under 35 U.S.C. §102. Therefore, Appellant urges the Board to reverse the examiner's rejections under 35 U.S.C. §102 of claims 1-11.

Further, Harish, alone or in combination with Kuznetzov, fails to disclose or suggest limitations recited in pending claims 12-16. Therefore, Harish, alone or in combination with Kuznetzov, cannot be used to establish the required prima facie case of obviousness under 35 U.S.C. §103. Therefore, Appellant urges the Board to reverse the examiner's rejections under 35 U.S.C. §103 of claims 12-16.

Respectfully submitted,

Jed W. Caven
Caven & Aghevli LLC
Attorney for Applicants



By:
Jed W. Caven
Registration No. 40,551
(720) 841-9544

Date: November 1, 2006

APPENDIX A

Claims

1. A virtual storage system for mapping virtual storage segments of differing sizes to storage locations, comprising:

an agent coupled to a host, the agent having volatile memory for storing a first table, the table having entries to map the virtual storage segments to the storage locations; and

a controller coupled to the agent, the controller having non-volatile memory for storing a second table, the controller intermittently causing contents of the first table to be replaced by contents of the second table,

whereby during an input/output (I/O) operation, the host accesses one of the entries in the first table to determine one of the storage locations.

2. The system of claim 1, wherein the second table identifies an alternate storage location within the storage locations.

3. The system of claim 2, wherein the second table further includes a bitmap having entries that correspond to blocks of data stored within the alternate storage location.

4. The system of claim 1, further comprising an alternate storage container comprising alternate storage locations of the storage location correlating to the virtual storage segments.

5. The system of claim 4, wherein an I/O operation accesses information on both the storage location and the alternative storage location.

6. The system of claim 5 wherein a bitmap designates blocks at the alternative storage location to use for the I/O operation.

7. A system for mapping a virtual disk segment to a storage location within a storage device, such that a host queries said system to determine said storage location for input/output operations, said system comprising:

a first table having a first table entry mapping the virtual disk segment to the storage location;

a second table having a second table entry corresponding to said storage location and to an alternate storage location, and block bitmap information identifying blocks of data having differing sizes within the alternate storage location;

a plurality of variables indicating states of an entry in the first table or the second table;

an offset for the entry, wherein the offset includes a logic unit number identifier and a block identifier;

a first memory to store the first table; and

a second memory to store the second table.

8. The system of claim 7, wherein said first memory is a volatile memory.

9. The system of claim 7, wherein said second memory is a non-volatile memory.

10. The system of claim 7, wherein the states include a no-write state.

11. The system of claim 7, wherein the states include an error state.

12. A method for performing an input/output operation on a virtual storage segment defined by a first table that maps a storage segment to a first storage location, the method comprising:

turning off input/output operations at the first storage location;

identifying portions of the virtual storage segment to be effected during a write operation;

storing a record of the identified portions at a second table and not at the first table; and

writing to a second storage location, whereby the writing operation occurs at portions of the second storage location associated with the identified portions.

13. The method of claim 12, wherein the turning off step includes activating an invalid state.

14. The method of claim 12, wherein a subsequent read operation for the virtual segment occur at portions of the first storage location not included in the identified portions and the portions of the second storage location associated with the identified portions.

15. The method of claim 14, wherein the first table is stored by an agent and during the read operation, the record of the identified portions is sent to the agent.

16. The method of claim 15, wherein the mapping between the virtual storage segment and first storage location is contained in numerous first tables, each of the first table stored by a different agent.

Evidence Appendix

None

Related Proceedings Appendix

None